CLAIMS

1. A semiconductor memory device comprising:

a non-volatile main storage memory including a storage region consisting of a plurality of storage capacity units which are composed of a data region in a first storage capacity and management region;

an address management information storage part for storing address management information of said main storage memory;

a non-volatile control memory for storing a writing completion flag table which is provided to said main storage memory every second storage capacity unit and consists of writing completion flags placed when data writing is completed; and

a control part for performing read/write control for said main storage memory in accordance with a direction of data read/write from a host and for performing update control for said address management information storage part and said control memory.

2. The semiconductor memory device according to claim 1, wherein

said second storage capacity unit is a cluster size, and

said control memory records the writing completion flag table consisting of writing completion flags of at least one bit for every cluster size prescribed by a file system of the host.

3. The semiconductor memory device according to claim 1, wherein

said second storage capacity unit is a sector size, and

said control memory records the writing completion flag table consisting of writing completion flags of at least one bit for every sector size prescribed by a file system of the host.

4. The semiconductor memory device according to claim 1, further comprises:

said second storage capacity unit is a physical block size, and

said control memory records the writing completion flag table consisting of writing completion flags of at least one bit for every capacity of N number of physical blocks in said main storage memory.

5. The semiconductor memory device according to claim 1, wherein

said control memory has higher writing-rate than that of said main storage memory.

6. The semiconductor memory device according to claim 1, wherein

said control part composes a memory map of the writing completion flag table at initialization or factory shipment based on a preliminarily stored second storage capacity unit.

7. The semiconductor memory device according to claim 1, wherein

said control part composes a memory map of the writing completion flag table at initialization or factory shipment based on a second storage capacity unit transferred from the host.

8. The semiconductor memory device according to claim 1, wherein

said main storage memory is a multi-valued NAND flash memory.

9. The semiconductor memory device according to claim 1, wherein

said address management information storage part

includes: a physical region management table for storing conditions every storage capacity unit of said main storage memory; and an address conversion table for converting an address designated by a file system of the host into an address of a storage capacity unit of said main storage memory.

10. The semiconductor memory device according to claim 1, wherein

said control memory is a ferroelectric random access memory (FeRAM).

11. The semiconductor memory device according to claim 1, wherein

said control memory is a magnetic random access memory (MRAM).

12. The semiconductor memory device according to claim 1, wherein

said control memory is an ovonic unified memory (OUM).

13. The semiconductor memory device according to claim 1, wherein

said control memory is a resistance RAM (RRAM).